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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/567,510	NAGAI, HIDEO	
	Examiner	Art Unit	
	Hoang-Quan Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *35-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *35-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/31/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on August 31, 2007 was filed after the mailing date of the Non-Final Office Action on April 27, 2007. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Amendment

Applicant's amendment dated July 25, 2007 is acknowledged. Currently, claims 35 – 45 are pending in light of the amendment, in which no claim was amended, claims 1 – 34 were cancelled, no claim was withdrawn, and claims 35 – 45 were added has been entered of record.

Response to Arguments

Applicant's arguments filed July 25, 2007 is acknowledged and is responded as follows.

Applicant has cancelled numerous claims, which included claim 29, for which was objected to. Due to cancellation of claim 29, the objection of claim 29 is moot. Also included was claim 15, for which was rejected under 35 U.S.C. § 112. Due to cancellation of claim 15, the rejection of claim 25 is moot.

Applicant's arguments, see pgs. 6 – 9, with respect to claims 35 – 45 have been fully considered but they are not fully persuasive in view of the following reasons.

In response to Applicant's arguments on pg. 7, Applicant submits that Ohtuka et al. does not teach a first and second power supply terminals formed on the main surface of the base substrate, which faces away from a multiplayer epitaxial structure. Ohtuka discloses only one power supply terminal 5 as seen in fig. 1. The Examiner respectfully disagrees and would like to draw Applicant's attention to fig. 1 of Ohtuka and the previous Office Action mailing date of April 27, 2007. The Examiner would like to point out to the Applicant that nowhere in claim 5 rejection, which the limitation is now integrated into claim 35, did the Examiner cited ref. no. 5 of Ohtuka, pointing to a power supply terminal. In the previous Office Action, the Examiner cited a first and second power supply terminals to be one of the connections of ref. nos. 16a – 16c. As clearly shown in fig. 1 of Ohtuka, once the transistors, which are ref. nos. 16a – 16c are switched on, it acts as a power source, thus considered as a power terminal for each LED, ref. nos. 10a – 10c. Furthermore, assuming arguendo, if ref. nos. 16a – 16c are reasonably construed as power terminals, they are not facing away from a multiplayer epitaxial structure. The Examiner respectfully disagrees and would like to point out to the Applicant that the power terminals are still facing away from a multilayer epitaxial structure. For instance, but not limited to, the top surface of ref. nos. 14a – 14c where it connects to ref. nos. 16a – 16c are facing away from the multilayer epitaxial structure. The Examiner recognizes that Applicant's first and second power terminals are located on the bottom of the substrate, which are facing away from the multiplayer epitaxial

layer. However, the claimed limitation does not distinguish vertical position, whether the power terminals are on top or bottom of the base substrate or multilayer epitaxial structure.

In response to Applicant's arguments on pg. 8, Applicant suggests that Ohtuka does not disclose a structure including a through hole included in a base substrate 3, it is found partially persuasive. Therefore, the rejection is withdrawn. However, upon further consideration, a new ground(s) of rejection is made below.

In response to Applicant's remarks regarding the phosphor extending over the second electrodes and only a portion of the exposed light emitting layer and that the silicon oxide covers the sides of the light emitting layers, it is found persuasive. Therefore, the rejection is withdrawn. However, upon further consideration, a new ground(s) of rejection is made below.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 38 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for the first conductive layer is a n-type semiconductor layer and the second conductive layer is a p-type semiconductor layer, does not reasonably provide enablement for claim 38's limitations of the opposite doping layers (see Applicant's specification of U.S. Patent App. Pub. No. 2006/0284195

A1, par. 0082). The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to swap layers of conductivities (p vs n type dopants) the invention commensurate in scope with these claims.

The Examiner presumes that Applicant wanted first conductive layer to be n type while the second conductive layer to be p type, in order to agree as set forth in the specification, the figs. and claim 35 for which claim 38 depends from.

Claim 43 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for a Ni/Au thin film ref. no. 20, does not reasonably provide enablement for Ni/An thin film as claimed in claim 43. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to claim an element "An" part of the thin film of the invention commensurate in scope with these claims.

The Examiner presumes that Applicant wanted to claim a Ni/Au thin film, as found in Applicant's specification of U.S. Patent App. Pub. No. 2006/0284195 A1, par. 0083.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 35 – 36 and 38 – 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagai et al. (U.S. Patent App. Pub. No. 2006/0180818 A1), hereinafter as Nagai, and in further view of Durocher et al. (U.S. Patent No. 6,614,103 B1), hereinafter as Durocher and in further view of Baretz et al. (U.S. Patent No. 6,600,175 B1), hereinafter as Baretz.

Regarding claim 35, figs. 1A – 2B of Nagai teaches a semiconductor light emitting device (ref. no. 2) comprising:

a base substrate (ref. no. 4);

a multilayer epitaxial structure includes a first conductive layer (ref. no. 14), a second conductive layer (ref. no. 18) and a light emitting layer (ref. no. 16) that is formed between the first conductive layer and the second conductive layer (as seen in fig. 2A), the multilayer epitaxial structure being formed on the base substrate in such a manner that the first conductive layer is positioned closer to the base substrate than the second conductive layer is (as seen in fig. 2A);

a first electrode (ref. no. 26) that is formed on the first conductive layer (as seen in fig. 2A);

a second electrode (ref. nos. 20, 22, and/or 24) that is formed on the second conductive layer (as seen in fig. 2A);

a first power supply terminal and a second power supply terminal that are formed on a main surface of the base substrate which faces away from the multilayer epitaxial structure (par. 0054 teaches that there is an anode and cathode on ref. nos. 6C and 6D,

as seen in figs. 1A – 1B for which are equated to a first and second power supply terminals; ref. no. 24 are the anodes and cathodes of ref. nos. 6C and 6D, and they are facing away from the multiplayer epitaxial structure, for instance, the upper surface is facing away from the multiplayer epitaxial structure; The Examiner recognizes that Applicant's first and second power terminals are located on the bottom of the substrate, which are facing away from the multiplayer epitaxial layer. However, the claimed limitation does not distinguish vertical position, whether the power terminals are on top or bottom of the base substrate or multilayer epitaxial structure.).

But Nagai does not teach the following limitations whereas fig. 12 of Durocher teaches that it is known in the art to provide:

a first conductive member (one of portion of the pair of ref. nos. 37 or 49) including a first through hole (ref. no. 51, e.g., fig. 5) that is provided in the base substrate (ref. no. 41, as seen in fig. 12), and electrically connecting the first electrode and the first power supply terminal (ref. no. 47 provides power, see col. 5, lines 14 – 16 and col. 9, lines 29 – 31);

a second conductive member (one other portion of the pair of ref. nos. 37 or 49) including a second through hole (ref. no. 51, e.g., fig. 5) that is provided in the base substrate (ref. no. 41, as seen in fig. 12), and electrically connecting the second electrode and the second power supply terminal (ref. no. 47 provides power, see col. 5, lines 14 – 16 and col. 9, lines 29 – 31).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the invention of Nagai with the conductive through holes

of Durocher, in order to provide power through the substrate. It is proper to combine Nagai and Durocher because they both teach analogous art relating to LED packaging.

But Nagai does not teach the following limitations whereas fig. 5 of Baretz teaches it is known in the art to provide:

a phosphor film (ref. no. 63) that covers a main surface of the multilayer epitaxial structure (ref. no. 41) which faces away from the base substrate (as seen in fig. 5), and every side surface of the multilayer epitaxial structure from a layer including the main surface to include at least the light emitting layer (as seen in fig. 5).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the invention of Nagai with the phosphor film of Baretz, in order to emit white light at a second relatively longer wave length (col. 12, lines 18 – 24). It is proper to combine Nagai and Baretz because they both teach analogous art relating to LED.

Regarding claim 36, Nagai, Durocher and Baretz teaches the semiconductor light emitting device of Claim 35, Nagai teaches wherein the multilayer epitaxial structure is formed on the base substrate leaving a space along each edge of a main surface of the base substrate which faces the multilayer epitaxial structure (as seen in fig. 1B, there is a space around the borders of ref. no. 2 of its LEDs); and

the first through hole and the second through hole are provided in a peripheral portion of the base substrate, the peripheral portion corresponding to the space (it would have been obvious to provide the through holes at each respective ends of ref.

nos. 6C and 6D with the teachings of Baretz, so that power can be delivered to the anode and out from the cathode from below the substrate).

Regarding claim 38, Nagai, Durocher and Baretz teaches the semiconductor light emitting device of Claim 35, Nagai teaches wherein the first conductive layer is a p-type semiconductor layer (see 35 U.S.C. § 112 rejection; par. 0045), and the second conductive layer is an n-type semiconductor layer (see 35 U.S.C. § 112 rejection; par. 0045).

Regarding claim 39, Nagai, Durocher and Baretz teaches the semiconductor light emitting device of Claim 38, Nagai teaches wherein a main surface of the n-type semiconductor layer which faces away from the light emitting layer is uneven so as to improve light extraction efficiency (as seen in fig. 2A, inherent based on structure as shown in the fig., see note 1 below).

Note 1: A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In essence, apparatus claims cover what a device is, not what a device does. See MPEP § 2114.

Regarding claim 40, Nagai, Durocher and Baretz teaches the semiconductor light emitting device of Claim 35 wherein the multilayer epitaxial structure is formed through

epitaxial growth, on a single-crystal substrate different from the base substrate, and transferred from the single-crystal substrate to the base substrate (see note 1 below).

Note 1: The recited limitation is drawn to a process by which the product is made. Even though product by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product by process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. Such product by process limitation does not structurally distinguish over the cited prior art. See MPEP § 2113.

In the instant case, multiplayer epitaxial structure formation would not result in a structural difference, because the process does not limit the final structure. Therefore, it does not distinguish from prior art.

Regarding claim 41, Nagai, Durocher and Baretz teaches the semiconductor light emitting device of Claim 40, wherein the multilayer epitaxial structure is transferred to the base substrate in such a manner that a last epitaxially-grown layer having grown on the single-crystal substrate is positioned closer to the base substrate than a first epitaxially-grown layer is (see note 1 of claim 40 rejection).

Regarding claim 42, Nagai, Durocher and Baretz teaches the semiconductor light emitting device of Claim 35, Nagai teaches wherein the base substrate is a SiC substrate (par. 0042).

Claims 43 – 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagai, Durocher and Baretz as applied to claim 35 above, and further in view of Camras et al. (U.S. Patent App. Pub. No. 2002/0093023 A1), hereinafter as Camras.

Regarding claim 43, Nagai, Durocher and Baretz teaches the semiconductor light emitting device of Claim 35, but Nagai, Durocher and Baretz do not teach the following limitation whereas fig. 3A of Camras teaches wherein the epitaxial structure has an uneven p-electrode surface as a second conductive layer (ref. no. 118). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the device of Nagai, Durocher and Baretz with the uneven electrode of Camras, in order to provide electrical contact to provide a voltage to the light emitting layer (par. 0037) and for current spreading and optical transparency (par. 0042). It is proper to combine Nagai, Durocher, Baretz, and Camras because they all teach analogous art relating to LED.

Regarding claim 44, Nagai, Durocher, Baretz, and Camras teaches the semiconductor light emitting device of Claim 43, Camras teaches wherein a plurality of

depressions is formed on a surface of the p-electrode surface (as seen in fig. 3A) to improve light extraction efficiency (par. 0042).

Regarding claim 45, Nagai, Durocher, Baretz, and Camras teaches the semiconductor light emitting device of Claim 43, Camras teaches wherein a Ni/Au thin film (par. 0038) and an ITO transparent electrode (par. 0042, teaches that ref. no. 118 can also be transparent depending on optical transparency, and ITO electrode is widely known material in the art to use for transparent electrode, see Andriessen of U.S. Patent App. Pub. No. 2002/0153830 A1) from the p-electrode.

Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nagai, Durocher and Baretz as applied to claim 35 above, and further in view of Ohtuka et al. (WIPO Patent App. Pub. No. WO/058726 A1), hereinafter as Ohtuka.

Regarding claim 37, Nagai, Durocher and Baretz teaches the semiconductor light emitting device of Claim 35, but Nagai, Durocher and Baretz do not teach the following limitation whereas figs. 1, 7, 11, and 18 of Ohtuka teaches further comprising:

a metal reflective film (ref. nos. 9a – 9c) that is sandwiched between the multilayer epitaxial structure (ref. nos. 10a – 10c) and the base substrate (ref. no. 3).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the invention of Nagai, Durocher and Baretz with the metal reflective film of Ohtuka, in order to provide reflection of light to a set direction. It

is proper to combine Nagai, Durocher, Baretz, and Ohtuka because they all teach analogous art relating to LED.

Claims 35 – 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durocher, and in further view of Baik et al. (U.S. Patent No. 2004/0108511 A1), hereinafter as Baik, and in further view of Baretz.

Regarding claim 35, fig. 12 of Durocher teaches a semiconductor light emitting device comprising:

a base substrate (ref. no. 41);

a multilayer epitaxial structure (col. 7, lines 23 – 40).

a first power supply terminal and a second power supply terminal (one of ref. no. 47 as seen in fig. 12) that are formed on a main surface of the base substrate which faces away from the multilayer epitaxial structure (on the bottom of ref. no. 41 as seen in fig. 12);

a first conductive member (one of portion of the pair of ref. nos. 37 or 49) including a first through hole (ref. no. 51, e.g., fig. 5) that is provided in the base substrate (ref. no. 41, as seen in fig. 12), and electrically connecting the first electrode (one of ref. no. 61) and the first power supply terminal (one of ref. no. 47 provides power, see col. 5, lines 14 – 16 and col. 9, lines 29 – 31);

a second conductive member (one other portion of the pair of ref. nos. 37 or 49) including a second through hole (ref. no. 51, e.g., fig. 5) that is provided in the base

substrate (ref. no. 41, as seen in fig. 12), and electrically connecting the second electrode (other ref. no. 61) and the second power supply terminal (other ref. no. 47 provides power, see col. 5, lines 14 – 16 and col. 9, lines 29 – 31).

But Durocher does not explicitly provide the details of the multiplayer epitaxial structure whereas fig. 2 of Baik teaches it is known in the art to provide a multiplayer epitaxial structure includes a first conductive layer (ref. no. 24), a second conductive layer (ref. no. 28) and a light emitting layer (ref. no. 26) that is formed between the first conductive layer and the second conductive layer (as seen in fig. 2), the multilayer epitaxial structure being formed on the base substrate (ref. no. 39) in such a manner that the first conductive layer is positioned closer to the base substrate than the second conductive layer is (as seen in fig. 2);

a first electrode (ref. no. 31) that is formed on the first conductive layer (as seen in fig. 2);

a second electrode (ref. no. 33) that is formed on the second conductive layer (as seen in fig. 2).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the invention of Durocher with the LED structure of Baik, in order to provide an alternative LED structure design to emit light. It is proper to combine Durocher and Baik because they both teach analogous art relating to LED.

But Durocher does not teach the following limitations whereas fig. 5 of Baretz teaches it is known in the art to provide:

a phosphor film (ref. no. 63) that covers a main surface of the multilayer epitaxial structure (ref. no. 41) which faces away from the base substrate (as seen in fig. 5), and every side surface of the multilayer epitaxial structure from a layer including the main surface to include at least the light emitting layer (as seen in fig. 5).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the invention of Durocher (e.g., LED, substrate) with the phosphor film and housing structure of Baretz, in order to emit white light at a second relatively longer wave length (col. 12, lines 18 – 24). It is proper to combine Durocher and Baretz because they both teach analogous art relating to LED.

Regarding claim 36, Durocher, Baik and Baretz teaches the semiconductor light emitting device of Claim 35, Durocher and Baretz teaches wherein the multilayer epitaxial structure is formed on the base substrate leaving a space along each edge of a main surface of the base substrate which faces the multilayer epitaxial structure (as seen in fig. 12 of Durocher, where on the left or right side, there is spacing above ref. no. 41 where the LEDs do not exist; as seen in fig. 5 of Baretz, where on the left or right side, there is spacing above ref. no. 42 where the LEDs do not exist); and

the first through hole and the second through hole are provided in a peripheral portion of the base substrate, the peripheral portion corresponding to the space (as seen in fig. 12 of Durocher or fig. 5 of Baretz where interconnects or leads are formed in the peripheral portions).

Regarding claim 37, Durocher, Baik and Baretz teaches the semiconductor light emitting device of Claim 35, fig. 2 of Baik teaches further comprising:

a metal reflective film (ref. nos. 35 and 37; par. 0038) that is sandwiched between the multilayer epitaxial structure (everything above ref. no. 37) and the base substrate (ref. no. 39; as seen in fig. 2).

Regarding claim 38, Durocher, Baik and Baretz teaches the semiconductor light emitting device of Claim 35, wherein the first conductive layer is a p-type semiconductor layer (see 35 U.S.C. § 112 rejection; par. 0036), and the second conductive layer is an n-type semiconductor layer (see 35 U.S.C. § 112 rejection; par. 0036).

Regarding claim 39, Durocher, Baik and Baretz teaches the semiconductor light emitting device of Claim 38, Baik teaches wherein a main surface of the n-type semiconductor layer which faces away from the light emitting layer is uneven (as seen in fig. 2, the left side of ref. no. 24 is uneven created by a cavity, the surface is facing away from the light emitting layer, such that it's outside of light emitting layer view, i.e., vertical view) so as to improve light extraction efficiency (see note 1 below).

Note 1: A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In essence, apparatus claims cover what a device is, not what a device does. See MPEP § 2114.

Regarding claim 40, Durocher, Baik and Baretz teaches the semiconductor light emitting device of Claim 35 wherein the multilayer epitaxial structure is formed through epitaxial growth, on a single-crystal substrate different from the base substrate, and transferred from the single-crystal substrate to the base substrate (see note 1 below).

Note 1: The recited limitation is drawn to a process by which the product is made. Even though product by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product by process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. Such product by process limitation does not structurally distinguish over the cited prior art. See MPEP § 2113.

In the instant case, multiplayer epitaxial structure formation would not result in a structural difference, because the process does not limit the final structure. Therefore, it does not distinguish from prior art.

Regarding claim 41, Durocher, Baik and Baretz teaches the semiconductor light emitting device of Claim 40, wherein the multilayer epitaxial structure is transferred to the base substrate in such a manner that a last epitaxially-grown layer having grown on the single-crystal substrate is positioned closer to the base substrate than a first epitaxially-grown layer is (see note 1 of claim 40 rejection).

Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Durocher, Baik and Baretz as applied to claim 35 above, and further in view of Furukawa et al. (U.S. Patent App. Pub. No. 2002/0149298 A1), hereinafter as Furukawa.

Regarding claim 42, Durocher, Baik and Baretz teaches the semiconductor light emitting device of Claim 35, but Durocher, Baik, and Baretz does not teach wherein the base substrate is a SiC substrate. However, Durocher teaches that the base substrate (ref. no. 41), can be made from flexible carrier, glass circuit board or the like (col. 5, lines 17 – 31). Furukawa teaches that it is known in the art to provide wherein the base substrate is a SiC substrate (par. 0773). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the invention of Durocher, Baik, and Baretz with the substrate material of Furukawa, in order to provide an alternative substrate material. It is proper to combine Durocher, Baik, Baretz, and Furukawa because they both teach analogous art relating to LED structure and the substrate materials.

Claims 43 – 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durocher, Baik and Baretz as applied to claim 35 above, and further in view of Camras.

Regarding claim 43, Durocher, Baik and Baretz teaches the semiconductor light emitting device of Claim 35, but Durocher, Baik and Baretz do not teach the following limitation whereas fig. 3A of Camras teaches wherein the epitaxial structure has an uneven p-electrode surface as a second conductive layer (ref. no. 118). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the device of Durocher, Baik and Baretz with the uneven electrode of Camras, in order to provide electrical contact to provide a voltage to the light emitting layer (par. 0037) and for current spreading and optical transparency (par. 0042). It is proper to combine Durocher, Baik, Baretz, and Camras because they all teach analogous art relating to LED.

Regarding claim 44, Durocher, Baik, Baretz, and Camras teaches the semiconductor light emitting device of Claim 43, Camras teaches wherein a plurality of depressions is formed on a surface of the p-electrode surface (as seen in fig. 3A) to improve light extraction efficiency (par. 0042).

Regarding claim 45, Durocher, Baik, Baretz, and Camras teaches the semiconductor light emitting device of Claim 43, Camras teaches wherein a Ni/Au thin film (par. 0038) and an ITO transparent electrode (par. 0042, teaches that ref. no. 118 can also be transparent depending on optical transparency, and ITO electrode is widely known material in the art to use for transparent electrode, see Andriessen of U.S. Patent App. Pub. No. 2002/0153830 A1) from the p-electrode.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. WO 2005/013365 A2 is the PCT version of Nagai (U.S. Patent App. Pub. No. 2006/0180818 A1).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

This action is a **final rejection** and is intended to close the prosecution of this application. Applicant's reply under 37 CFR 1.113 to this action is limited either to an appeal to the Board of Patent Appeals and Interferences or to an amendment complying with the requirements set forth below.

If applicant should desire to appeal any rejection made by the examiner, a Notice of Appeal must be filed within the period for reply identifying the rejected claim or claims appealed. The Notice of Appeal must be accompanied by the required appeal fee.

If applicant should desire to file an amendment, entry of a proposed amendment after final rejection cannot be made as a matter of right unless it merely cancels claims or complies with a formal requirement made earlier. Amendments touching the merits of the application which otherwise might not be proper may be admitted upon a showing a good and sufficient reasons why they are necessary and why they were not presented earlier.

A reply under 37 CFR 1.113 to a final rejection must include the appeal from, or cancellation of, each rejected claim. The filing of an amendment after final rejection, whether or not it is entered, does not stop the running of the statutory period for reply to the final rejection unless the examiner holds the claims to be in condition for allowance. Accordingly, if a Notice of Appeal has not been filed properly within the period for reply, or any extension of this period obtained under either 37 CFR 1.136(a) or (b), the application will become abandoned.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoang-Quan Ho whose telephone number is (571) 272-8711. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HQH/
Hoang-Quan Ho
Junior Examiner
September 19, 2007

Andy Huynh
Primary Examiner